



# UNITED STATES PATENT AND TRADEMARK OFFICE

col

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,450	04/13/2004	Shi-dong Zhou	X-1530 US	4699

24309 7590 06/14/2005

XILINX, INC  
ATTN: LEGAL DEPARTMENT  
2100 LOGIC DR  
SAN JOSE, CA 95124

EXAMINER

TON, MY TRANG

ART UNIT PAPER NUMBER

2816

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/823,450

Applicant(s)

ZHOU ET AL.

Examiner

My-Trang N. Ton

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-23 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 24-28 is/are rejected.
- 7) ☒ Claim(s) 5-12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.



**MY-TRANG NUTON  
PRIMARY EXAMINER**

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Flannagan (U.S Patent No. 6,031,408).

Flannagan discloses in Fig. 6 a square law clamping circuit including:

a single transistor (136) connected between the I/O pin (121) and ground potential (Vss) and having a gate (gate of 136); and

means for controlling (130-135 and 141) the conductive state of the single transistor (136) in response to an enable signal (OE) as recited in claim 1.

Regarding claim 2: the means for controlling (130-135 and 141) comprises a select circuit (130-135 and 141) having an input terminal to receive the enable signal (OE) and having an output terminal coupled to the gate of the single transistor (136).

Regarding claim 3: the select circuit (130-135 and 141) turn on the single transistor (136) to sink current from the I/O pin (121) in response to an asserted state (HIGH state) of the enable signal (OE), and turn off the single transistor (136) to disable the clamp circuit in response to a de-asserted state (LOW state) of the enable signal (OE).

Regarding claim 4: the enable signal (OE) is asserted (HIGH state) when the IC device operates in a first system that requires the I/O pin (121) to be clamped during a voltage overshoot condition (when 136 ON) and the enable signal (OE) is de-asserted (LOW state) when the IC device operates in a second system (132 OFF, 136 OFF) that requires the I/O pin (121) to be tri-stated (when no power supply connection).

The method recited in claims 24-27 are similarly rejected as above claims: one discharge transistor (136), I/O pin (121), ground potential (Vss), a select circuit (130-135 and 141), an enable signal (OE), asserting state (HIGH state), de-asserting state (LOW state).

Regarding claim 28, the limitation “the first system comprises a Peripheral Component Interface system” is seen to define intended use. The clamping circuit of Flannagan is capable of comprising a Peripheral Component Interface system. *In re* Tuominen, 213 USPQ 89 (CCPA 1982) & *In re* Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).

### ***Allowable Subject Matter***

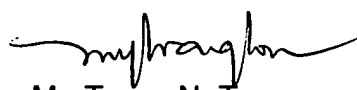
Claims 5-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: the combination of “a voltage detection circuit coupled to the I/O pin ...” and “a voltage level shifter circuit having a power terminal connected to the I/O pin ...” as recited in claim 5, “a PMOS transistor” in combination with “a voltage level shifter circuit” as recited in claim 9.

Claims 13-23 are allowable over the prior art of record. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "a voltage detection circuit coupled to the I/O pin..." and "a voltage level shifter circuit having a power terminal connected to the I/O pin..." in combination with "a discharge circuit" as recited in claim 13; "a PMOS transistor" and "a voltage level shifter circuit" in combination with "a discharge circuit" as recited in claim 19.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton  
Primary Examiner  
Art Unit 2816

6/9/05